WHAT IS CLAIMED IS:

1. A memory device, comprising:

a memory core for storing data, said memory core having a plurality of control inputs and a datapath restricted from simultaneous read and write operations; and

interface circuitry coupled to an interconnect structure which carries control and data information, said control information including read and write commands, said data information including read and write data information, said interface circuitry being coupled to said control inputs of said memory core to manage memory core operations and to said datapath of said memory core to transfer data information between said interconnect structure and said memory core, said interface circuitry including

a write control buffer to store a write command, and

a write data buffer to store write data information, wherein when said interface circuitry receives a read command after a write command, said write control buffer stores said write command and said write data buffer stores write data information for said write command so that said interface circuitry may perform said read command on said memory core prior to performing said write command on said memory core.

2. The memory device of claim 1 wherein said write data buffer is configured to retire said write data information in response to any operation code signal other than one associated with processing of a read command to the memory device.

3. The memory device of claim 1 wherein said write data buffer is configured to retire said write data information in response to a dedicated retire control signal.

4. The memory device of claim 1 wherein said write data buffer is configured to retire said write data information in the absence of any operation code signal.

5. The memory device of claim 1 wherein said memory device is configured to identify correspondence between a write command within said write control buffer and a memory read command.

6. The memory device of claim 1 wherein said memory device is configured to substantially equalize at said interface circuitry the time to store write information and retrieve read information.

7. The memory device of claim 6 wherein said memory device is configured to delay the issuance of a write control command at said memory core.

8. A memory system, comprising:

a communication channel;

a master memory device connected to said communication channel, said master memory device configured to generate a memory write command with associated write information followed by a memory read command; and

a slave memory device connected to said communication channel, said slave memory device configured to process said memory read command at a slave device memory core prior to processing said memory write information.

9. The memory system of claim 8 wherein said memory system includes:

a write control buffer to store said memory write command; and

a write data buffer to store said write information, said write information being loaded into said slave device memory core when a read is not being processed or when a read is abandoned.

10. The memory system of claim 9 wherein said write data buffer is configured to retire said memory write information in response to any operation code signal other than one associated with processing a read command to the memory device.

11. The memory system of claim 9 wherein said write data buffer is configured to retire said memory write information in response to a dedicated retire control signal.

12. The memory system of claim 9 wherein said write data buffer is configured to retire said write data information in the absence of any operation code signal.

13. The memory system of claim 9 wherein said write control buffer and said write data buffer are positioned in said slave memory device.

14. The memory system of claim 9 wherein said write control buffer and said write data buffer are positioned in said master memory device.

15. The memory system of claim 8 wherein said master memory device is configured to generate a plurality of memory write commands followed by any operation code other than a read or write to the target slave device and said memory read command to a particular slave device, said slave memory device being configured to respond thereto by processing said memory read command prior to completing the processing of said plurality of memory write commands without causing a column resource conflict at said slave device memory core.

16. The memory system of claim 8 wherein said master memory device is configured to generate separated memory write commands in order to prevent data overrun in buffers of a particular slave memory device.

17. The memory system of claim 8 wherein said master memory device is configured to generate memory write commands separated by other operation commands in order to prevent data overrun in buffers of a particular slave memory device.

18. The memory system of claim 8 wherein said master memory device is configured to generate memory write commands separated by memory write commands to different slave memory devices in order to prevent data overrun in buffers of a particular slave memory device.

19. The memory system of claim 8 wherein said master memory device is configured to generate memory write commands separated by memory read commands in order to prevent data overrun in buffers of a particular slave memory device.

20. The memory system of claim 9 wherein said slave memory device is configured to identify correspondence between said memory write command within said write control buffer and said memory read command.

21. The memory system of claim 8 wherein said slave memory device is configured to substantially equalize at said interface circuitry the time to store said write information and retrieve read information.

22. The memory system of claim 21 wherein said slave memory device is configured to delay the issuance of a write control command at said slave device memory core.

23. A method of operating a memory system with a master memory device connected to a slave memory device, said method comprising the steps of:

generating with said master memory device a memory write command with associated write information followed by a memory read command;

buffering said memory write command and write information in response to said memory read command;

processing said memory read command at said slave memory device; and

handling said memory write information at said slave memory device after said processing step.

24. The method of claim 23 wherein said buffering step includes the steps of:

transporting said write information into a write data buffer; and

retiring said write information from said write data buffer after said processing step so as to facilitate loading of said write information into a memory core of said slave memory device.

25. The method of claim 24 wherein said retiring step is performed in response to an operation code associated with control signals of said processing step.

26. The method of claim 24 wherein said retiring step is performed in response to a dedicated retire control signal that is generated independently of said memory read command.

27. The method of claim 24 wherein said retiring step is performed in response to a new memory write command.

28. The method of claim 23 wherein said buffering step is performed in said slave memory device.

29. The method of claim 23 wherein said buffering step is performed in said master memory device.

30. The method of claim 23 wherein said generating step includes the step of generating with said master memory device a plurality of memory write commands followed by any operation code other than a read or write to the target slave device and said memory read command to a particular slave device, such that said memory read command is processed at said slave memory device before completion of said plurality of write commands without causing a column resource conflict at a memory core of said slave memory device.

31. The method of claim 23 wherein said generating step includes the step of generating separated memory write commands in order to prevent data overrun in buffers of a particular slave memory device.

32. The method of claim 23 wherein said generating step includes the step of generating memory write commands separated by a no operation command in order to prevent data overrun in buffers of a particular slave memory device.

33. The method of claim 23 wherein said generating step includes the step of generating memory write commands separated by memory write commands to different slave memory devices in order to prevent data overrun in buffers of a particular slave memory device.

34. The method of claim 23 wherein said generating step includes the step of generating memory write commands separated by memory read commands to different slave memory devices in order to prevent data overrun in buffers of a particular slave memory device.

35. The method of claim 23 further comprising the step of identifying correspondence between said memory write command as buffered during said buffering step and said memory read command and in response thereto loading said write information into a memory core of said slave memory during said processing step.

36. The method of claim 23 further comprising the step of substantially equalizing at interface circuitry of said slave device the time to store said write information and said read information.

37. The method of claim 36 wherein said equalizing step includes the step of delaying the issuance of said write command.